REMARKS

All Claims Define Allowable Subject Matter

Claims 1 and 3 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,822,346 to Arai (hereinafter "Arai"). Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Arai as applied to claims 1 and 3.[1] These rejections are respectfully traversed for at least the following reasons.

At page 6 of the Amendment previously filed on February 28, 2005 in this application, Applicants explained that Arai does not disclose, or even suggest, a current mirror circuit configured in the manner required by independent claim 1 and its dependent claims 2 and 3. Applicants explained that a current mirror circuit, as can be understood with reference to, for example, the URL http://en.wikipedia.org/wiki/Current_mirror, includes a pair of transistors, with the gate (or base) of each transistor being connected to the gate (or base) of the other transistor. The Examiner noted that the printout of this webpage was not included with the previous filing, but that he had printed out a copy via the supplied link. To ensure that the record is complete in this regard, Applicants are attaching a copy of this 1 page document to the instant amendment as Exhibit A.

In the previously-filed Amendment, Applicants explained that circuit elements 10, 11, 14, 15 and 16 of Arai do not constitute a current mirror source as recited in the combination of independent claim 1. Applicants explained, for example, that element 14 of Arai relates to a constant current circuit controlled by D/A converter 10, whereas a current mirror circuit provides mirror currents in two lines, as explained in the above-discussed attached Exhibit A. Applicants

[1] Applicants understand that the Examiner intended to refer to claim 2 here in the rejection under 35 U.S.C. § 103(a). If Applicants' understanding is incorrect, clarification is requested in the next Office Communication.

respectfully submit that elements 14 and 15 of Arai do not provide mirror currents in their respective lines.

In response, the Examiner points out, at page 4 of the Final Office Action, his interpretation of what a "current mirror" is semantically. The Examiner indicates that a current mirror "is a circuit which provides [sources or sinks] constant current." According to the Examiner, "[t]his is done by supplying a reference current [first line] and supply or sink current [second line]."

Applicants do not agree that the current source of Arai is disclosed as including a current mirror arrangement to any extent. Applicants respectfully submit that while a "current mirror circuit" can be used as a "current source," it is not always a current source. In addition, a constant current source does not always include a current mirror circuit arrangement, as asserted by the Final Office Action. A current mirror circuit is understood to those skilled in the relevant art as being a circuit having a very specific circuit arrangement, as previously discussed, that reflects the input current in the output. As an example of this understanding, Applicants attach, as Exhibit B, a title page and pages 269-271 of a text entitled "Analysis and Design of Analog Integrated Circuits" by Gray et al. (3rd Edition). Applicants specifically refer to page 271 of this text in this regard.

In addition, the Examiner concedes at page 4 of the Final Office Action that "Yes, Arai has not shown well known details of constant current source." However, the Examiner then alleges that "one of ordinary skill in the art knows that when constant current is supplied ... it MUST have two transistors for constant current supply to work. So by definition Arai has two transistors."

Applicants respectfully traverse the Examiner's assertion in this regard at least because it is understood by those having still in the relevant art that a current source can be made of a single transistor. As an example of this general understanding, Applicants attach, as Exhibit C, pages 1-5 of a publication entitled "The FET Constant-Current Source/Limiter" (Siliconix March 10, 1997).

Accordingly, it is clear from the foregoing discussion and the three documents referred to above that a "constant current source" (as disclosed in Arai) and a "current mirror" are not "one and the same thing" as asserted by the Final Office Action at page 5. As a result, Applicants respectfully submit that Arai does not teach at least the current mirror features specifically described in independent claim 1.

Even further, Applicants respectfully submit that Arai does not show the specific connections of the "first current mirror circuit" of independent claim 1 having, for example, "two parallel lines, said laser diode being connected with one of the two parallel lines" and "a control circuit connected with the other of the two parallel lines, said control circuit controlling the current flowing in this line in accordance with a potential of this line, this potential comprising a steady DC component when reading data ... and this potential comprising a drive signal component added to said DC component when writing data."

Applicants respectfully submit that each of the current sources 14, 15 and 16 disclosed in Arai are likely made of a single FET, control signals being input to their gates respectively. There is surely no disclosure, or even a suggestion, of using a current mirror circuit arrangement in Arai.

Accordingly, Applicants respectfully assert that the rejections under 35 U.S.C. §§ 102(b) and 103(a) should be withdrawn because Arai does not teach, or even suggest, each feature of

independent claim 1. As pointed out in MPEP § 2131, "[t]o anticipate a claim, the reference must teach every element of the claim." Thus, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. Verdegaal Bros. v. Union Oil Co. Of California, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987)." Similarly, MPEP § 2143.03 instructs that "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 409 F.2d 981, 180 USPQ 580 (CCPA 1974)." Accordingly, Applicants respectfully submit that independent claim 1 is in condition for allowance. In addition, dependent claims 2-3 are also in condition for allowance at least because of their dependence on independent claim 1.

CONCLUSION

In view of the foregoing, Applicants respectfully request reconsideration of this application, withdrawal of all rejections, and the timely allowance of the pending claims. Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicants' undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0573. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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Dated: September 23, 2005 By: _____

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